Training Course on Advanced Digital VLSI Design and Verification

Professional Development Training Course Outline

Category	Engineering	**Duration**	10 Days
Base Fee	$3,000 USD	**Delivery Mode**	Online / On-site Hybrid

Course Introduction

Introduction

Training Course on Advanced Digital VLSI Design and Verification equips participants with the latest methodologies and industry practices in Very-Large-Scale Integration (VLSI) design, focusing on RTL design, functional verification, timing closure, and design-for-test (DFT) strategies. In a fast-evolving semiconductor landscape driven by AI acceleration, 5G SoCs, and edge computing, this course is vital for engineers aiming to stay ahead in digital hardware design. Participants will learn how to create scalable, power-efficient, and performance-optimized digital systems using Verilog, SystemVerilog, UVM, SVA, and EDA tools such as Synopsys Design Compiler, Cadence Genus, Mentor Questa, and VCS.

This hands-on training blends theoretical foundations with practical case studies in SoC design, FPGA prototyping, and ASIC verification. The curriculum spans advanced RTL coding, logic synthesis, formal verification, clock domain crossing, and power-aware verification. By the end of the course, attendees will master both the design and verification flow for complex VLSI systems, ensuring design integrity, functional correctness, and first-time-right silicon success.

Programme Curriculum

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Course Objectives

1. Understand the digital VLSI design flow from RTL to GDSII.
2. Apply RTL design principles using Verilog and SystemVerilog.
3. Master UVM (Universal Verification Methodology) for scalable testbenches.
4. Analyze and solve timing closure and static timing analysis issues.
5. Implement power-aware design techniques with UPF/CPF.
6. Apply Design-for-Testability (DFT) methodologies like scan insertion.
7. Conduct formal and assertion-based verification (SVA).
8. Explore SoC design challenges including bus protocols and IP integration.
9. Address clock domain crossing (CDC) and metastability risks.
10. Use FPGA for rapid prototyping of digital designs.
11. Automate testbench generation and coverage analysis.
12. Gain experience with EDA tools for synthesis and simulation.
13. Prepare for tape-out and silicon validation processes.

Organizational Benefits

1. Accelerate product development with skilled VLSI professionals.
2. Improve design quality and reduce verification cycles.
3. Minimize post-silicon debug and costly re-spins.
4. Enhance innovation through internal ASIC/FPGA capabilities.
5. Reduce outsourcing costs for chip verification.
6. Strengthen IP development and reuse strategy.
7. Build in-house SoC design and prototyping expertise.
8. Promote cross-functional collaboration in chip design projects.
9. Ensure compliance with latest industry standards (e.g., IEEE 1800).
10. Develop a pipeline of high-performance hardware design talent.

Target Participants

- VLSI Design Engineers
- ASIC/FPGA Design and Verification Engineers
- SoC and RTL Designers
- Embedded Systems Engineers
- Electrical & Electronics Engineers
- Computer Engineers and Researchers
- Postgraduate Students in Digital Design

- Technical Leads and Chip Architects

Course Outline

Module 1: VLSI Design Overview

- Moore's Law and Scaling Trends
- VLSI Design Flow: Frontend to Backend
- ASIC vs. FPGA Design
- EDA Tools and Design Environments
- Case Study: 5G SoC Development Cycle

Module 2: RTL Design with Verilog/SystemVerilog

- Combinational and Sequential Logic
- FSM and Pipelining Structures
- Parameterization and Reusability
- Coding for Synthesis vs. Simulation
- Case Study: UART RTL Design

Module 3: Synthesis and Constraints

- Logic Synthesis Process
- Timing Constraints (SDC Files)
- Optimization Techniques
- Technology Libraries
- Case Study: ALU Synthesis with Design Compiler

Module 4: Static Timing Analysis (STA)

- Setup and Hold Time Violations
- Clock Skew and Jitter Analysis
- Path-Based vs. Graph-Based Analysis
- Timing Reports Interpretation
- Case Study: Resolving STA Violations in Pipeline

Module 5: Functional Verification with SystemVerilog

- Data Types and Constructs
- Interfaces and Clocking Blocks
- Constrained Random Testing
- Functional Coverage
- Case Study: FIFO Verification

Module 6: UVM-Based Verification

- UVM Architecture and Components
- Factory and Configuration Patterns
- TLM Communication

- Reusable Testbench Creation
- Case Study: UVM Testbench for Memory Controller

Module 7: Assertion-Based Verification (ABV)

- SystemVerilog Assertions (SVA)
- Immediate vs. Concurrent Assertions
- Coverage with Assertions
- Debugging with Assertions
- Case Study: Assertion Checking in Cache Controller

Module 8: Formal Verification Techniques

- Equivalence Checking
- Property Checking
- Formal Tool Flow
- Benefits and Limitations
- Case Study: Register File Formal Validation

Module 9: Clock Domain Crossing (CDC) Design

- CDC Issues and Metastability
- Synchronization Techniques
- CDC Verification Tools
- Linting and Static Analysis
- Case Study: Multi-Clock SoC

Module 10: Low Power Design and Verification

- Dynamic vs. Static Power
- Power Gating and Clock Gating
- UPF/CPF Integration
- Power-Aware Simulation
- Case Study: Low Power IoT Processor

Module 11: Design-for-Testability (DFT)

- Scan Chains and ATPG
- Boundary Scan (JTAG)
- BIST Techniques
- Fault Simulation
- Case Study: DFT in Automotive Microcontrollers

Module 12: FPGA Design and Prototyping

- RTL to Bitstream Flow
- FPGA Constraints and Placement
- IP Cores and Soft Processors
- FPGA Debug Tools (ILA, VIO)

- Case Study: Prototyping a RISC-V Core

Module 13: SoC Integration and IP Reuse

- On-Chip Bus Protocols (AXI, AHB, APB)
- IP Wrappers and Interfaces
- SoC Verification Strategies
- Memory Subsystems
- Case Study: SoC Design for Embedded Vision

Module 14: Advanced Verification Techniques

- Coverage-Driven Verification
- Regression Testing and CI Pipelines
- Functional Safety and ISO 26262
- Portable Stimulus Standards
- Case Study: Safety Verification in Automotive SoCs

Module 15: Tape-Out and Post-Silicon Validation

- Design Sign-Off Checklist
- Netlist to GDSII
- Silicon Bring-Up and Debug
- Lab Setup for Validation
- Case Study: First-Time-Right ASIC Tape-Out

Training Methodology

This course employs a participatory and hands-on approach to ensure practical learning, including:

- Interactive lectures and presentations.
- Group discussions and brainstorming sessions.
- Hands-on exercises using real-world datasets.
- Role-playing and scenario-based simulations.
- Analysis of case studies to bridge theory and practice.
- Peer-to-peer learning and networking.
- Expert-led Q&A sessions.
- Continuous feedback and personalized guidance.

Register as a group from 3 participants for a Discount

Send us an email: info@fineskilltrainingcenter.org or call *+254769199797*

Certification

Upon successful completion of this training, participants will be issued with a globally- recognized certificate.

Tailor-Made Course

We also offer tailor-made courses based on your needs.

Key Notes

a. The participant must be conversant with English.

b. Upon completion of training the participant will be issued with an Authorized Training Certificate

c. Course duration is flexible and the contents can be modified to fit any number of days.

d. The course fee includes facilitation training materials, 2 coffee breaks, buffet lunch and A Certificate upon successful completion of Training.

e. One-year post-training support Consultation and Coaching provided after the course.

f. Payment should be done at least a week before commence of the training, to Fineskill Training Center account, as indicated in the invoice so as to enable us prepare better for you.

Upcoming Scheduled Sessions

Start Date	End Date	Location	Price
23 Nov 2026	04 Dec 2026	Online	$2,000
23 Nov 2026	04 Dec 2026	Physical	$3,000
23 Nov 2026	04 Dec 2026	Physical	$6,000
23 Nov 2026	04 Dec 2026	Physical	$6,000
23 Nov 2026	04 Dec 2026	Physical	$12,000
23 Nov 2026	04 Dec 2026	Physical	$9,000
23 Nov 2026	04 Dec 2026	Physical	$12,000
23 Nov 2026	04 Dec 2026	Physical	$12,000

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