Training Course on Field-Programmable Gate Array (FPGA) Design and High-Level Synthesis (HLS)

Professional Development Training Course Outline

Category	Engineering	**Duration**	10 Days
Base Fee	$3,000 USD	**Delivery Mode**	Online / On-site Hybrid

Course Introduction

Introduction

The Field-Programmable Gate Array (FPGA) Design and High-Level Synthesis (HLS) Training Course is a comprehensive, industry-aligned program designed to equip engineers, designers, and embedded system professionals with the tools and knowledge needed to leverage FPGAs for high-performance computing, embedded systems, and rapid hardware prototyping. As industries embrace AI acceleration, edge computing, real-time data processing, and 5G/6G communication, FPGAs have emerged as flexible, low-latency, reconfigurable hardware solutions that deliver unmatched performance.

Training Course on Field-Programmable Gate Array (FPGA) Design and High-Level Synthesis (HLS) combines traditional RTL design methods (using VHDL/Verilog) with modern high-level synthesis (HLS) using tools like Xilinx Vitis HLS and Intel HLS Compiler, enabling rapid design cycles from C/C++ to FPGA logic. Participants will learn timing optimization, resource utilization, IP integration, debugging, and hardware-software co-design for applications in AI, machine learning, automotive systems, signal processing, and IoT devices. Case studies from real-world projects will illustrate best practices in deploying FPGA solutions for complex workloads.

Programme Curriculum

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Course Objectives

1. Understand FPGA architecture and programmable logic fundamentals
2. Write synthesizable code in VHDL and Verilog
3. Develop FPGA designs using Xilinx Vivado and Intel Quartus Prime
4. Apply High-Level Synthesis (HLS) using C/C++ for hardware acceleration
5. Optimize timing, power, and area in logic design
6. Integrate IP cores using AXI and Avalon interfaces
7. Implement pipelining, parallelism, and loop unrolling
8. Perform functional simulation and timing verification
9. Deploy FPGA-based accelerators for AI and ML workloads
10. Design embedded systems using FPGA SoCs (Zynq/Arria)
11. Debug designs using SignalTap and Integrated Logic Analyzer (ILA)
12. Perform FPGA implementation for real-time signal processing
13. Explore applications in 5G/6G, automotive, and IoT systems

Organizational Benefits

1. Accelerate product development cycles using reconfigurable hardware
2. Enable hardware acceleration for compute-intensive applications
3. Reduce dependency on ASIC development with FPGA prototypes
4. Improve system performance through hardware-software co-design
5. Gain expertise in HLS to reduce verification time and effort
6. Enhance in-house capabilities for IP development and reuse
7. Leverage FPGA for edge AI, DSP, and real-time analytics
8. Foster cross-functional skillsets between hardware and software teams
9. Ensure compliance with modern toolchains and synthesis standards
10. Position your team for innovation in telecom, medical, and defense sectors

Target Participants

- FPGA Engineers and Digital Design Engineers
- Embedded Systems Developers
- Hardware Engineers and System Architects

- R&D Engineers working on AI, signal processing, or 5G
- Graduate students and academic researchers in Electronics
- Automotive, Telecom, and Aerospace Engineers

Course Outline

Module 1: Introduction to FPGA Technology

- What is an FPGA and how it works
- FPGA vs ASIC vs Microcontroller
- Basic architecture: CLBs, BRAM, DSP slices
- FPGA vendors overview: Xilinx, Intel, Lattice
- Case Study: FPGA in automotive radar systems

Module 2: VHDL and Verilog Essentials

- Syntax and structure of VHDL/Verilog
- RTL modeling and testbenches
- Combinational vs sequential logic
- FSM (Finite State Machine) design
- Case Study: Traffic light controller in Verilog

Module 3: Development Tools and Environment Setup

- Xilinx Vivado toolchain
- Intel Quartus Prime overview
- Simulators: ModelSim, Vivado Simulator
- Project structure and constraints management
- Case Study: Vivado project for LED blinking

Module 4: High-Level Synthesis (HLS) with C/C++

- Concept of HLS and when to use it
- Writing C/C++ for hardware synthesis
- Loop unrolling and pipelining
- Toolchains: Vitis HLS, Intel HLS Compiler
- Case Study: FIR filter design in Vitis HLS

Module 5: Timing and Resource Optimization

- Timing analysis and slack
- Critical path minimization
- Register balancing and retiming
- Logic area estimation
- Case Study: Optimizing ALU performance

Module 6: FPGA IP Integration

- Xilinx IP catalog and custom IP creation
- AXI and Avalon interface protocols
- Clocking and reset strategies
- Block design using Vivado IP Integrator
- Case Study: UART IP integration

Module 7: Simulation and Verification

- Behavioral vs structural simulation
- Testbench development in HDL
- Functional vs timing simulation
- Assertion-based verification
- Case Study: Verification of PWM controller

Module 8: Embedded Systems with FPGA SoCs

- Zynq and Intel SoC FPGA architecture
- Processing System (PS) vs Programmable Logic (PL)
- Bare-metal and Linux-based development
- Memory-mapped peripheral interfacing
- Case Study: Zynq-based motor controller

Module 9: Real-Time DSP on FPGA

- FIR and IIR filter implementation
- FFT and convolution engines
- Fixed vs floating-point arithmetic
- Data buffering and throughput management
- Case Study: DSP core for software-defined radio

Module 10: FPGA for AI and Machine Learning

- CNN acceleration using HLS
- Quantization-aware design for AI inference
- Custom neural network layers on FPGAs
- Frameworks: Vitis AI, OpenVINO
- Case Study: Face detection on FPGA

Module 11: Debugging and Analysis Tools

- SignalTap and Vivado ILA setup
- Triggering, probing, and waveform capture
- On-chip debugging techniques
- Performance monitoring and timing analyzer
- Case Study: Real-time debugging of SPI interface

Module 12: System-Level Design and Integration

- Multi-clock domain design
- Clock domain crossing techniques
- System partitioning and modular design
- Communication protocols: SPI, I2C, CAN
- Case Study: FPGA as sensor hub in autonomous vehicles

Module 13: Power Management in FPGA Designs

- Dynamic power vs static power
- Clock gating and power islands
- Power estimation tools
- Low-power design methodologies

- Case Study: Power-optimized wearable device

Module 14: Security and Reliability in FPGA

- Bitstream encryption and secure boot
- Redundancy and fault tolerance
- Soft error mitigation techniques
- Secure firmware updates
- Case Study: FPGA security in aerospace systems

Module 15: Future Trends and Industry Use-Cases

- FPGAs in 6G wireless infrastructure
- FPGA cloud instances (AWS F1, Azure NP)
- 3D FPGA architectures and chiplets
- HLS and AI compilers evolution
- Case Study: FPGA-based acceleration in data centers

Training Methodology

This course employs a participatory and hands-on approach to ensure practical learning, including:

- Interactive lectures and presentations.
- Group discussions and brainstorming sessions.
- Hands-on exercises using real-world datasets.
- Role-playing and scenario-based simulations.
- Analysis of case studies to bridge theory and practice.
- Peer-to-peer learning and networking.
- Expert-led Q&A sessions.
- Continuous feedback and personalized guidance.

Register as a group from 3 participants for a Discount

Send us an email: info@fineskilltrainingcenter.org or call *+254769199797*

Certification

Upon successful completion of this training, participants will be issued with a globally- recognized certificate.

Tailor-Made Course

We also offer tailor-made courses based on your needs.

Key Notes

a. The participant must be conversant with English.

b. Upon completion of training the participant will be issued with an Authorized Training Certificate

c. Course duration is flexible and the contents can be modified to fit any number of days.

d. The course fee includes facilitation training materials, 2 coffee breaks, buffet lunch and A Certificate upon successful completion of Training.

e. One-year post-training support Consultation and Coaching provided after the course.

f. Payment should be done at least a week before commence of the training, to Fineskill Training Center account, as indicated in the invoice so as to enable us prepare better for you.

Upcoming Scheduled Sessions

Start Date	End Date	Location	Price
23 Nov 2026	04 Dec 2026	Online	$2,000
23 Nov 2026	04 Dec 2026	Physical	$3,000
23 Nov 2026	04 Dec 2026	Physical	$6,000
23 Nov 2026	04 Dec 2026	Physical	$6,000
23 Nov 2026	04 Dec 2026	Physical	$12,000
23 Nov 2026	04 Dec 2026	Physical	$9,000
23 Nov 2026	04 Dec 2026	Physical	$12,000
23 Nov 2026	04 Dec 2026	Physical	$12,000

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