# Training Course on High-Speed Digital System Design

Professional Development Training Course Outline

| | | | |
|---|---|---|---|
| **Category** | Engineering | **Duration** | 10 Days |
| **Base Fee** | $3,000 USD | **Delivery Mode** | Online / On-site Hybrid |

## Course Introduction

### Introduction

In today’s rapidly evolving digital landscape, high-speed digital system design is fundamental to achieving optimal performance in cutting-edge applications such as data centers, telecommunication systems, IoT devices, and embedded systems. Training Course on High-Speed Digital System Design offers engineers and system designers a comprehensive guide to signal integrity, timing analysis, PCB layout, jitter mitigation, and power integrity—the core aspects that ensure reliable and high-performance digital systems.

Participants will gain in-depth knowledge through industry-relevant case studies, interactive labs, and real-world design scenarios. This course bridges theoretical foundations with practical implementations, equipping learners with the advanced design skills needed to innovate and troubleshoot high-frequency digital systems in a world driven by speed, efficiency, and precision.

## Programme Curriculum

### Training Course on High-Speed Digital System Design

### Introduction

In today’s rapidly evolving digital landscape, high-speed digital system design is fundamental to achieving optimal performance in cutting-edge applications such as data centers, telecommunication systems, IoT devices, and embedded systems. Training Course on High-Speed Digital System Design offers engineers and system designers a comprehensive guide to signal integrity, timing analysis, PCB layout, jitter mitigation, and power integrity—the core aspects that ensure reliable and high-performance digital systems.

Participants will gain in-depth knowledge through industry-relevant case studies, interactive labs, and real-world design scenarios. This course bridges theoretical foundations with practical implementations, equipping learners with the advanced design skills needed to innovate and troubleshoot high-frequency digital systems in

a world driven by speed, efficiency, and precision.

**Course duration**

10 Days

## Course Objectives

1. Understand the fundamentals of signal integrity analysis in high-speed circuits.
2. Perform timing budget analysis and understand setup and hold time violations.
3. Design for electromagnetic compatibility (EMC) and regulatory compliance.
4. Analyze and mitigate crosstalk, reflections, and ringing in transmission lines.
5. Implement multi-gigabit transceiver designs for FPGA and ASIC systems.
6. Master high-speed PCB layout techniques and routing strategies.
7. Evaluate and improve power distribution networks (PDN).
8. Utilize SI/PI simulation tools like HyperLynx and Ansys SIwave effectively.
9. Integrate low-jitter clock distribution networks in high-speed systems.
10. Conduct bit error rate (BER) testing and eye diagram analysis.
11. Develop high-speed interfaces using DDR, PCIe, USB 3.0, and Ethernet.
12. Apply SI/PI co-design principles for concurrent engineering success.
13. Enhance design validation and debugging using high-bandwidth oscilloscopes.

## Organizational Benefits

1. Improve time-to-market with faster design verification cycles.
2. Enhance product reliability and robustness through optimized designs.
3. Reduce field failures and RMA costs via predictive analysis.
4. Boost productivity with upskilled engineering teams.
5. Adopt best practices for cost-effective PCB design.
6. Maintain competitive edge through cutting-edge design tools.
7. Increase team efficiency with simulation-driven workflows.
8. Align designs with global compliance and EMI standards.
9. Enable innovation in next-gen digital products.
10. Foster cross-functional collaboration in hardware-software integration.

## Target Participants

- Hardware Engineers
- Signal Integrity Engineers
- Embedded System Designers
- PCB Layout Engineers
- FPGA/ASIC Developers
- System Architects
- R&D Engineers
- Test and Validation Engineers
- Graduate Students in Electronics
- Product Development Teams

## Course Outline

### Module 1: Introduction to High-Speed Digital Systems

- Definitions and key concepts
- High-speed vs. low-speed design
- Key challenges in digital systems
- Overview of industry trends
- Case Study: Ethernet PHY failures

### Module 2: Signal Integrity Fundamentals

- Transmission line theory
- Impedance and reflections
- Termination techniques
- Propagation delay
- Case Study: DDR4 SI bottlenecks

### Module 3: Timing Analysis and Budgeting

- Setup and hold times
- Clock skew and jitter
- Timing budget allocation
- Synchronous vs asynchronous timing
- Case Study: FPGA timing failures

### Module 4: PCB Stack-up and Layer Planning

- Stack-up design principles
- Controlled impedance routing
- Differential pair design
- Layer assignments for noise control
- Case Study: EMI issues from poor stack-up

### Module 5: Crosstalk and Coupling Mitigation

- Near-end and far-end crosstalk
- Trace spacing and topology
- Shielding techniques
- Use of guard traces
- Case Study: USB3.0 cross-channel interference

### Module 6: Power Integrity (PI) Essentials

- PDN design and decoupling
- Voltage ripple analysis
- Target impedance methodology
- Ground bounce mitigation
- Case Study: Power noise in GPU designs

### Module 7: Simulation Tools and Techniques

- Introduction to SI/PI tools
- Pre-layout vs. post-layout simulation

- Time domain and frequency domain analysis
- Model extraction (IBIS, SPICE)
- Case Study: Simulation preventing field failure

**Module 8: Clocking and Jitter Management**

- Clock distribution networks
- PLLs and clock jitter
- Clock tree vs. clock mesh
- Clock skew analysis
- Case Study: High-speed ADC clocking issues

**Module 9: High-Speed Interface Design**

- PCIe Gen4/Gen5
- DDR3/DDR4/DDR5 memory interfaces
- USB 3.1 and USB 4
- 10G/40G/100G Ethernet PHY
- Case Study: PCIe link training failure

**Module 10: Routing High-Speed Signals**

- Routing differential pairs
- Length matching and skew control
- Serpentine routing techniques
- Vias and via stubs effects
- Case Study: HDMI signal distortion

**Module 11: Electromagnetic Compatibility (EMC)**

- Sources of EMI in digital systems
- Filtering and shielding techniques
- Layout strategies for EMC
- Compliance standards (FCC, CISPR)
- Case Study: Failing EMC certification

**Module 12: Eye Diagrams and Bit Error Rate Testing**

- Interpreting eye diagrams
- Jitter and noise margin analysis
- BER testing methods
- Eye mask templates
- Case Study: Eye diagram troubleshooting

**Module 13: Design Validation and Debugging**

- High-bandwidth oscilloscopes
- Time-domain reflectometry (TDR)
- Logic analyzers in validation
- Debugging intermittent failures
- Case Study: Debugging field returns

**Module 14: Co-Design and Cross-Domain Collaboration**

- Concurrent engineering principles
- SI/PI co-design flow
- Firmware and hardware alignment
- Design reviews and documentation
- Case Study: Embedded system co-design success

**Module 15: Future Trends in High-Speed Design**

- AI/ML in digital hardware design
- Silicon photonics and optical interconnects
- 3D IC and chiplet packaging
- Quantum-safe signaling techniques
- Case Study: Emerging chiplet platform

## Training Methodology

This course employs a participatory and hands-on approach to ensure practical learning, including:

- Interactive lectures and presentations.
- Group discussions and brainstorming sessions.
- Hands-on exercises using real-world datasets.
- Role-playing and scenario-based simulations.
- Analysis of case studies to bridge theory and practice.
- Peer-to-peer learning and networking.
- Expert-led Q&A sessions.
- Continuous feedback and personalized guidance.

**Register as a group from 3 participants for a Discount**

**Send us an email: info@fineskilltrainingcenter.org or call** *+254769199797*

***Certification***

*Upon successful completion of this training, participants will be issued with a globally- recognized certificate.*

***Tailor-Made Course***

*We also offer tailor-made courses based on your needs.*

**Key Notes**

**a.** The participant must be conversant with English.

**b.** Upon completion of training the participant will be issued with an Authorized Training Certificate

**c.** Course duration is flexible and the contents can be modified to fit any number of days.

**d.** The course fee includes facilitation training materials, 2 coffee breaks, buffet lunch and A Certificate upon successful completion of Training.

**e.** One-year post-training support Consultation and Coaching provided after the course.

**f.** Payment should be done at least a week before commence of the training, to Fineskill Training Center account, as indicated in the invoice so as to enable us prepare better for you.

## Upcoming Scheduled Sessions

| Start Date | End Date | Location | Price |
|---|---|---|---|
| **23 Nov 2026** | 04 Dec 2026 | Online | $2,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $3,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $6,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $6,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $12,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $9,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $12,000 |
| **23 Nov 2026** | 04 Dec 2026 | Physical | $12,000 |

Ready to enroll or request a customized program? Book online or contact us:

**Register Online Now**

Email: info@fineskilltrainingcenter.com | Website: www.fineskilltrainingcenter.com